IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A method of calculating critical area in an integrated circuit design, said method comprising:

inputting an integrated circuit design;

constructing a Vornoi diagram for a particular fault mechanism based on a layout of device shapes in said initial integrated circuit design;

associating variables with the positions of edges of said device shapes in said integrated circuit design; ~~and~~

associating cost functions of said variables with spacing between said edges in said integrated circuit design; and

~~wherein~~ defining said cost functions in terms of ~~calculate~~ critical area contributions of linear bisectors between said edges of said device shapes. ~~as the positions and length of said edges in said integrated circuit design change, and~~

wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges of said device shapes ~~in said integrated circuit design.~~, and

wherein a critical area contribution of a given linear bisector is proportional to a cross product of an x-y difference vector between normal vectors of planes of Vornoi cells which meet at said given linear bisector and an x-y difference vector representing a length of said given

linear bisector such that said critical area contribution of said given linear bisector is a function of said variables.

2. (Currently Amended) The method in claim 1, wherein said process of associating said cost functions comprises mapping points in said spacing between said edges of said device shapes in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges of said device shapes in said integrated circuit design, wherein said mapping forms said Voronoi cells.

3. (Currently Amended) The method in claim [[2]] 1, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables.

4. (Cancelled).

5. (Currently Amended) The method in claim [[4]] 1, wherein said ~~Voronoi~~ linear bisectors are defined by vertices at the ends of said ~~Voronoi~~ linear bisectors; and wherein said vertices are defined in terms of said variables.

6. (Currently Amended) A method of optimizing critical area in an integrated circuit design, said method comprising:

a) inputting an initial integrated circuit design and constructing a Vornoi diagram for a

particular fault mechanism based on a layout of device shapes in said initial integrated circuit design;

b) associating variables with the positions of edges of said device shapes in said integrated circuit design;

c) associating cost functions of said variables with spacing between said edges of said device shapes in said integrated circuit design,

wherein said cost functions are defined in terms of critical area contributions of linear bisectors between said edges of said device shapes and

wherein a critical area contribution of a given linear bisector is proportional to a cross product of an x-y difference vector between normal vectors of planes of Vornoi cells which meet at said given linear bisector and an x-y difference vector representing a length of said given linear bisector such that said critical area contribution of said given linear bisector is a function of said variables;

d) optimizing said positions and length of said edges of said device shapes in said integrated circuit design to reduce critical area contribution cost in a first direction across said integrated circuit design to produce a revised integrated circuit design by using a linear optimization algorithm; and

e) repeating steps b-d with said revised integrated circuit design in a second direction.

7. (Currently Amended) The method in claim 6, wherein said process of associating said cost functions comprises mapping points in said spacing between said edges of said device shapes in said integrated circuit design up to when the size of defects located at said points

~~triggers an electrical fault between said edges~~ of said device shapes ~~in said integrated circuit design~~, wherein said mapping forms said Voronoi cells.

8. (Currently Amended) The method in claim [[7]] 6, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables.

9. (Cancelled).

10. (Currently Amended) The method in claim [[9]] 6, wherein said ~~Voronoi~~ linear bisectors are defined by vertices at the ends of said linear ~~Voronoi~~ bisectors; and wherein said vertices are defined in terms of said variables.

11. (Currently Amended) The method in claim [[10]] 6, wherein said ~~cost function calculates~~ critical area contributions of said linear ~~Voronoi~~ bisectors change with changes in ~~as~~ said variables ~~change~~ as ~~the~~ a layout of said device shapes in said integrated circuit design changes during said optimizing.

12. (Currently Amended) A method of optimizing critical area in an integrated circuit design, said method comprising:

a) inputting an initial integrated circuit design and constructing a Vornoi diagram for a particular fault mechanism based on a layout of device shapes in said initial integrated circuit

design;

b) associating variables with the positions of edges of device shapes in said integrated circuit design;

c) associating cost functions of said variables with spacing between said edges of said device shapes in said integrated circuit design,

wherein said cost functions are defined in terms of critical area contributions of linear bisectors between said edges of said device shapes, ~~and~~

wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges of said device shapes ~~in said integrated circuit design~~, and

wherein a critical area contribution of a given linear bisector is proportional to a cross product of an x-y difference vector between normal vectors of planes of Vornoi cells which meet at said given linear bisector and an x-y difference vector representing a length of said given linear bisector such that said critical area contribution of said given linear bisector is a function of said variables;

d) optimizing said positions and lengths of said edges of said device shapes in said integrated circuit design to reduce critical area contribution cost in a first direction across said integrated circuit design to produce a revised integrated circuit design by using a linear optimization algorithm; and

e) repeating steps b-d with said revised integrated circuit design in a second direction.

13. (Currently Amended) The method in claim [[15]] 12, wherein said process of associating

said cost functions comprises mapping points in said spacing between said edges of said device shapes in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges of said device shapes in said integrated circuit design, wherein said mapping forms said Voronoi cells.

14. (Currently Amended) The method in claim [[16]] 12, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables.

15. (Cancelled).

16. (Currently Amended) The method in claim [[18]] 12, wherein said ~~Voronoi~~ linear bisectors are defined by vertices at the ends of said ~~Voronoi~~ linear bisectors; and wherein said vertices are defined in terms of said variables.

17. (Currently Amended) The method in claim [[19]] 16, wherein said ~~cost function calculates~~ critical area contributions of said linear ~~Voronoi~~ bisectors change with changes in ~~as~~ said variables ~~change~~ as ~~the~~ a layout of said device shapes in said integrated circuit design changes during said optimizing.

18-23 (Cancelled).

24. (Currently Amended) A program storage device readable by computer, tangibly embodied a program of instructions executable by said computer for performing a method of calculating critical area in an integrated circuit design, said method comprising:

inputting an integrated circuit design;

constructing a Vornoi diagram for a particular fault mechanism based on a layout of device shapes in said initial integrated circuit design;

associating variables with the positions of edges of said device shapes in said integrated circuit design; ~~and~~

associating cost functions of said variables with spacing between said edges in said integrated circuit design; and

~~wherein~~ defining said cost functions in terms of ~~calculate~~ critical area contributions of linear bisectors between said edges of said device shapes, ~~as the positions and length of said edges in said integrated circuit design change, and~~

wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges of said device shapes ~~in said integrated circuit design.~~, and

wherein a critical area contribution of a given linear bisector is proportional to a cross product of an x-y difference vector between normal vectors of planes of Vornoi cells which meet at said given linear bisector and an x-y difference vector representing a length of said given linear bisector such that said critical area contribution of said given linear bisector is a function of said variables.

25. (Currently Amended) ~~The program storage device in claim [[29]] 24, wherein said~~ process of associating said cost functions comprises mapping points in said spacing between said edges of said device shapes in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges of said device shapes in said integrated circuit design, wherein said mapping forms said Voronoi cells.

26. (Currently Amended) The program storage device in claim [[30]] 24, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables.

27. (Cancelled).

28. (Currently Amended) The program storage device in claim [[32]] 24, wherein said ~~Voronoi~~ linear bisectors are defined by vertices at the ends of said ~~Voronoi~~ linear bisectors; and wherein said vertices are defined in terms of said variables.

29. (Currently Amended) The program storage device in claim [[33]] 24, wherein said ~~cost function calculates~~ critical area contributions of said linear ~~Voronoi~~ bisectors change with changes in ~~as~~ said variables ~~change~~ as ~~the~~ a layout of said device shapes in said integrated circuit design changes during said optimizing.

30. (Currently Amended) A system for calculating critical area in an integrated circuit

design, ~~said system comprising:~~

means for inputting an integrated circuit design and constructing a Vornoi diagram for a particular fault mechanism based on a layout of device shapes in said initial integrated circuit design;

means for associating variables with the positions of edges of said device shapes in said integrated circuit design; and

means for associating cost functions of said variables with spacing between said edges in said integrated circuit design;

wherein said cost functions are defined in terms of critical area contributions of linear bisectors between said edges of said device shapes, ~~and~~

wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges of said device shapes in said integrated circuit design, and

wherein a critical area contribution of a given linear bisector is proportional to a cross product of an x-y difference vector between normal vectors of planes of Vornoi cells which meet at said given linear bisector and an x-y difference vector representing a length of said given linear bisector such that said critical area contribution of said given linear bisector is a function of said variables.

31. (Original) A method of optimizing critical area in an integrated circuit design, said method comprising:

inputting an initial integrated circuit design;

constructing a Vornoi diagram for a particular fault mechanism based on a layout of device shapes in said initial integrated circuit design;

associating variables with the positions of edges of said device shapes in said integrated circuit design;

associating cost functions of said variables with spacing between said edges in said integrated circuit design;

defining said cost functions in terms of critical area contributions of linear bisectors between said edges of said device shapes,

wherein a critical area contribution of a given linear bisector is proportional to a cross product of an x-y difference vector between normal vectors of planes of Vornoi cells which meet at said given linear bisector and an x-y difference vector representing a length of said given linear bisector such that said critical area contribution of said given linear bisector is a function of said variables; and

optimizing said positions and length of said edges of said device shapes in said integrated circuit design to reduce critical area contribution cost in a first direction across said integrated circuit design to produce a revised integrated circuit design by using a linear optimization algorithm .

32. (Currently Amended) The method in claim [[37]] 31, wherein said process of associating said cost functions comprises mapping points in said spacing between said edges of said device shapes in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges of said device shapes in said integrated circuit

~~design, wherein said mapping forms~~ said ~~Voronoi cells~~.

33. (Currently Amended) The method in claim [[38]] 32, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables.

34. (Cancelled).

35. (Currently Amended) The method in claim [[40]] 31, wherein said linear ~~Voronoi~~ bisectors are defined by vertices at the ends of said linear ~~Voronoi~~ bisectors; and wherein said vertices are defined in terms of said variables.

36. (Currently Amended) The method in claim [[41]] 35, wherein said ~~cost function calculates~~ critical area contributions of said linear ~~Voronoi~~ bisectors change with changes in ~~as~~ said variables ~~change~~ as ~~the~~ a layout of said device shapes in said integrated circuit design changes during said optimizing.

37. (New) A method of optimizing critical area in an integrated circuit design, said method comprising:

constructing a Vornoi diagram for a particular fault mechanism based on a layout of device shapes in an integrated circuit design,

wherein said constructing of said Vornoi diagram comprises forming a plurality

of cells with boundaries that comprise linear bisectors between edges of said device shapes;

calculating a critical area contribution for each linear bisector,

wherein said critical contribution for said each linear bisector is proportional to a cross product of an x-y difference vector between normal vectors of planes which meet at said each linear bisector and an x-y difference vector representing a length of said each linear bisector such that said corresponding critical area contribution of said each linear bisector is a function of orientations and positions of said edges of said device shapes;

presenting said corresponding critical area contributions for each of said linear bisectors as costs; and,

using a linear optimization algorithm to modify said layout of said device shapes such that a sum of said costs for all of said linear bisectors is minimized.

38. (New) The method in claim 37, wherein said forming of said plurality of cells comprises mapping points in spacing between said edges of said device shapes up to when the size of defects located at said points triggers an electrical fault between said edges of said device shapes in said integrated circuit design.

39. (New) The method in claim 37, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors and wherein said vertices are defined in terms of said orientations and said positions of said edges of said device shapes.

40. (New) The method in claim 37, further comprising before said modifying, predicting

changes in said critical area contribution for each of said linear bisectors as a result of subsequent layout modifications.

41. (New) A program storage device readable by computer, tangibly embodied a program of instructions executable by said computer for performing a method of calculating critical area in an integrated circuit design, said method comprising:

constructing a Vornoi diagram for a particular fault mechanism based on a layout of device shapes in an integrated circuit design,

wherein said constructing of said Vornoi diagram comprises forming a plurality of cells with boundaries that comprise linear bisectors between edges of said device shapes;

calculating a critical area contribution for each linear bisector,

wherein said critical contribution for said each linear bisector is proportional to a cross product of an x-y difference vector between normal vectors of planes which meet at said each linear bisector and an x-y difference vector representing a length of said each linear bisector such that said corresponding critical area contribution of said each linear bisector is a function of orientations and positions of said edges of said device shapes;

presenting said corresponding critical area contributions for each of said linear bisectors as costs; and,

using a linear optimization algorithm to modify said layout of said device shapes such that a sum of said costs for all of said linear bisectors is minimized.

42. (New) The method in claim 41, wherein said forming of said plurality of cells comprises

mapping points in spacing between said edges of said device shapes up to when the size of defects located at said points triggers an electrical fault between said edges of said device shapes in said integrated circuit design.

43. (New) The method in claim 41, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors and wherein said vertices are defined in terms of said orientations and said positions of said edges of said device shapes.

44. (New) The method in claim 41, further comprising before said modifying, predicting changes in said critical area contribution for each of said linear bisectors as a result of subsequent layout modifications.